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Phase control algorithm for demodulation of binary phase-shift keying signals

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The purpose of this paper is to synthesize an algorithm for coherent digital demodulation of non-uniformly distributed radio signals with absolute two-position phase shift keying, which has a small computational complexity, and to develop a miniature low-power demodulator on its basis. The relevance of the study is determined by the absence of similar devices in the Russian radio electronic market. The algorithm is based on digital phase-locked-loop frequency control. Its basic idea is to retain the optimal amplitude ratio between the phase quadrature of the received signal using a proportional-integral-differential controller. A digital device with the stated technical characteristics was obtained as a result of the study.

Keywords: absolute phase-shift keying, demodulation, Costas circuit, phase-locked-loop, three-term controller, proportional-integral-differential controller, programmable logic, CORDIC algorithm

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Introduction

As is known, absolute binary phase-shift keying (BPSK) has the greatest noise resistance among other types of modulation [1]. This property makes its use especially advantageous in transmitting information in satellite television- and radio-broadcasting and telemetry. However, the use of this advantage is possible only in the case of providing precision coherent reception. The most widespread method of providing time synchronization is the Costas scheme [1]. In the feedback circuit, it uses the multiplier of quadratures as a frequency detector, the output of which sets the frequency of the voltage controlled generator (VCG). The block diagram of the Costas loop is shown in Fig. 1.

Nevertheless, the Costas loop has a number of shortcomings: firstly, this is an analog circuit, and its technical implementation is associated with difficulties in tuning which are characteristic of analog circuits. Secondly, the retention bandwidth is inversely proportional to the bandwidth of the loop filter [2], which increases the likelihood of cycle skip in difficult interference situations. Thirdly, the scheme has a tendency to the so-called inverse work [3], which is expressed in the erroneous mapping of the phase constellation points to the transmitted data in connection with an arbitrary initial state of the signal. As a result, this scheme is used only together with the application of preliminary bit synchronization, provided by means of antinoise coding, data addition with a correlation word or a preamble, which, in turn, further complicates the technical implementation of receiving-transmitting equipment.

The present paper discusses the algorithm and prototype of the device for demodulation of binary phase-shift keyed signals, devoid of the aforementioned shortcomings due to the use of the means of digital signal processing.

Demodulation algorithm

In the synthesis of the algorithm, it was decided to achieve its realizability in programmable logic integrated circuits (PLICs) of a small volume, up to 20,000 logical elements. The Costas scheme for BPSK, considered in

[5], which was subjected to a number of modifications, was taken as a prototype. Firstly, to input into the circuit, the input signal was pre-digitized. Secondly, in digital systems, a precision direct digital frequency synthesis (DDFS) device, implemented in PLICs using lookup tables, is an analog of a voltage-controlled generator. And, thirdly, to control the synthesizer in the feedback circuit, instead of the quadrature multiplier, a phase calculation and processing unit was implemented. The block diagram of the algorithm is presented in Fig. 2.

The calculation and processing of the phase are carried out by means of finding the arctangent of the amplitudes of the quadrature signals. In PLICs, this operation can be implemented through the CORDIC algorithm. Its result is a value lying in the range $[-\pi, \pi]$. This signal is a phase difference arising due to the frequency mismatch of the reference frequency generators of the receiver and transmitter, and undergoes jumps of p rad under the influence of the modulating information sequence. If the radio channel is approximated by additive white Gaussian noise, this signal can be described by the formula

$$\varphi'(t) = \frac{2\pi}{f_s} f'(t) + \pi C(t) + \theta. \quad (1)$$

Here $\varphi'(t)$ is the phase differential with respect to time, rad/s; f_s is the demodulator sampling frequency, Hz; $f'(t)$ is the differential of the carrier frequencies of the modulator (transmitter) and demodulator (receiver) with respect to time, Hz/s; $C(t)$ is the modulating information sequence; θ is additive white Gaussian noise, rad.

For the automatic phase synchronization of DDFS, it is necessary to eliminate modulation from this signal [4], which is realized by taking the absolute value of the difference between $\pi/2$ radians and the signal modulus. For this operation, there is the expression

$$\varphi_н = \left| \frac{\pi}{2} - |\varphi| \right|, \quad (2)$$

where φ is the initial value of the phase difference, rad; $\varphi_н$ is the normalized value of the phase difference, rad.

In this case, the jump-like changes caused by modulation are eliminated, but the dynamic range of the signal is narrowed to the interval $[0, \pi/2]$. Nevertheless, the resulting signal uniquely determines the amplitude ratio between the quadrature channels; therefore, after smoothing and low-pass filtering, it can be used as a feedback signal in the control circuit of DDFS. The bandwidth of the filter for smoothing this signal is chosen in accordance with the maximum admissible frequency difference of clock generators, which is determined by the mechanical and design features of the devices used. Finally, the filtered signal is subtracted from the threshold value $\varphi_ж$, which determines the

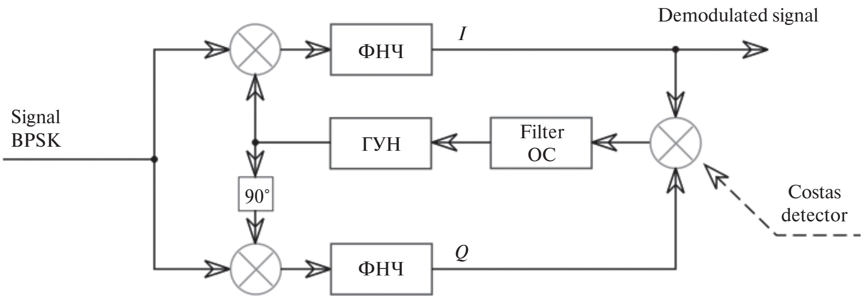

Figure 1. Costas circuit for demodulation of phase-shift keyed signals: *I* – common-mode signal; *Q* – quadrature signal; ФНЧ – low-pass filter; OC – feedback; 90° – phase-shifting unit; ГУН – voltage-controlled oscillator

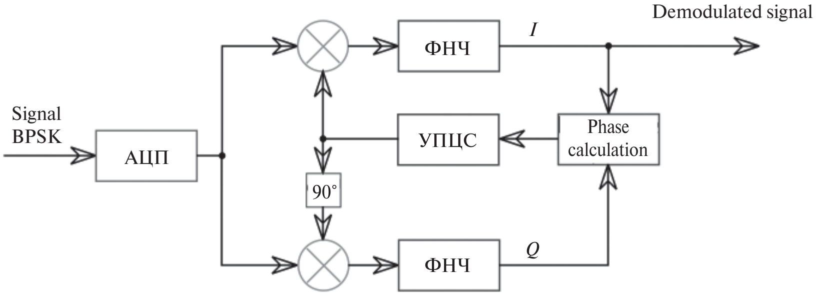

Figure 2. Functional diagram of the demodulation algorithm: АЦП – analog-to-digital converter

desired amplitude ratio between the quadrature signals, depending on the magnitude of the frequency disagreement and the signal-to-noise ratio. So, if the desired ratio is set to be 6 dB, then the average amplitude of the quadrature component, from which the information signal is taken (see Fig. 2), should be 4 times more than the average interference level in the channel. The result of the comparison with $\varphi_ж$ is the stabilization error signal of the phase e of the reference frequency generated by DDFS, which in turn is fed to the input of the proportional-integral-differential (PID) regulator, which produces the control signal for DDFS. The algorithm for computing and processing the phase is presented in Fig. 3.

Carrying out the research

Quality assessment was performed by laboratory and field tests of the developed device.

The experimental stand consisted of a binary phase-shift keyed-signal transmitter, a receiver constructed on the basis of the algorithm described above, and a spectrum analyzer. With the help of a spectrum analyzer, a preliminary radio monitoring of the environment was carried out, and the power density of the interferences was detected that fall into the working band of the receiving device. The power of the transmitted signal was conditioned by the design features of the transmitter and was 0.7 W. Thus, it is possible to determine the dependence of the received signal power on the distance between devices in the direct visibility conditions according to formula (3), known as the Friis equation:

$$P_R = P_T \frac{G_T G_R \lambda^2}{(4\pi d)^2}. \quad (3)$$

Here P_R is the power received from the receiving antenna, W; P_T is the power supplied to the transmitting antenna, W; G_T is the gain of the transmitting antenna; G_R is the gain factor of the receiving antenna; $\lambda = c/f$ is the wavelength, m; c is the speed of light in vacuum, m/s; f is the frequency, Hz; d is distance, m.

The technique of conducting experimental studies consisted in uniform removing the transmitter from the receiver fixed at the point where preliminary radio monitoring was conducted, calculating the signal-to-noise ratio based on the data on the distance between devices and the probability P_B of erroneous reception of a character as the ratio of the number of mistakenly received characters to the total number of characters received. The results of experimental studies were summarized in the graph of the dependence of P_B on the signal-to-noise ratio (Fig. 4b).

The theoretical estimate of the probability P_B of error when receiving binary phase-shift keyed signals can be obtained from the formula

$$P_B = \frac{1}{\sqrt{2\pi}} \int_{\sqrt{2E_b/N_0}}^{\infty} exp\left(-\frac{u^2}{2}\right) du. \quad (4)$$

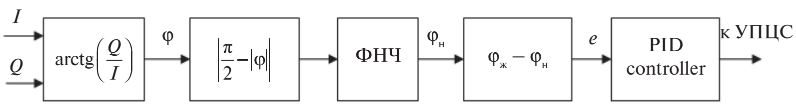

Figure 3. Functional diagram of the algorithm for computing and processing the phase:
$\mathrm{arctg}\left(\frac{Q}{I}\right)$ – trigonometric arctangent function; φ – initial value of the phase difference;
$\left|\frac{\pi}{2} - |\varphi|\right|$ – normalization operation

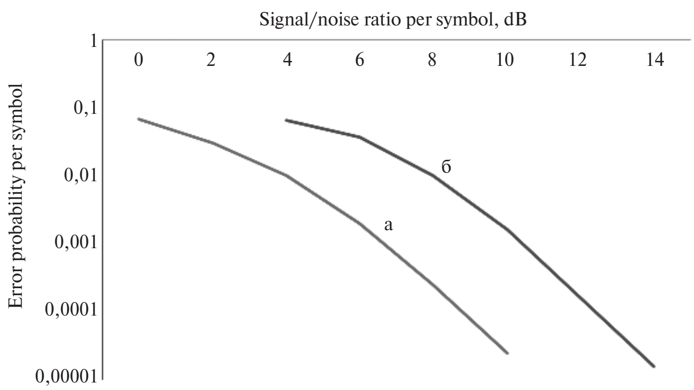

Figure 4. Dependence of the probability of incorrect P_B symbol reception on the signal-to-noise ratio resulting from: a – approximate calculation of the Gauss error integral; b – experimental studies

In expression (4), E_b is the signal energy per 1 bit of the received message, W; N_0 is the energy spectral noise density, W; $u = z - a_{(1,2)}/\sigma$; z is the value of the received signal; $a_{(1,2)}$ is the signal component of the received signal z when transmitting a binary symbol; σ is the noise variance. Expression (4) is called the Gaussian integral of errors and cannot be calculated analytically. The graph of the dependence of P_B on the signal-to-noise ratio, obtained by an approximate calculation of the Gaussian error integral, is shown in Fig. 4a. It should be noted that the estimate of P_B, obtained in this way, is reliable only if the conditional probability $P(z|s_{(1,2)})$ of receiving the transmitted binary symbol $s_{(1,2)}$ is known and is not equal to zero. In practical terms, this means that to achieve theoretical values of P_B, it is necessary to build an optimal coherent demodulator using correlators or coordinated filters, which in turn implies that the nature of the transmitted signal (the distribution density of the a priori probability $P(s_{(1,2)})$) should be known in advance.

Conclusion

The described demodulation algorithm was implemented on Intel's Cyclon IVE PLIC. The design, made in the Verilog hardware description language, had dimensions of 15,000 logical elements. With the wired connection of the receiver and transmitter through the step attenuator, it was found that the developed demodulator has a sensitivity of the input signal equal to –98 dBm (2 μV).

The main task posed in designing the described demodulator was to implement the Costas circuit on a digital element base, as well as to increase the capture bandwidth and the degree of noise immunity of the circuit so that the amount of the required computing resources was minimal. Besides, a mandatory property of the demodulator should be its ability to detect the transmitted signal without any information about the nature of the transmitted data.

As a result, the described algorithm was synthesized. In accordance with it, a prototype demodulator was developed that has a number of properties, including:

- the ability to maintain a known amplitude ratio between quadrature signals and thus uniquely detect the transmitted data, resulting in improved noise immunity, an increase in the band of admissible frequency disagreement between the frequencies of the received signal and the controlled synthesizer; a decrease of the likelihood of failure to monitor the phase in a difficult interfering environment;
- the ability to detect non-uniformly distributed data, from which it is possible to transfer informational messages with the prevailing number of zeros or ones, without additional bit synchronization through preambles or the sync word, which in turn removes restrictions from the transmitting device algorithm;
- realizability in programmable logic due to the absence of complex mathematical operations, which allows minimizing the number of resources used and increasing processing speed.

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